Direct-Coupled GaAs Monolithic IC Amplifiers

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ABSTRACT

A two-stage GaAs FET monolithic amplifier has been developed that exhibits a noise figure of 2dB and a gain of 20dB at frequencies from 0.3 to 1.5 GHz. The FET gate width is optimized to 1mm to lower the noise figure for a 50Ω signal source impedance. A direct-coupled scheme is used for chip size reduction. All the circuit elements such as FETs, Schottky diodes and resistors are fabricated by using selective ion-implantation for realizing a planar structure.

Introduction

Extensive development efforts are being directed in various laboratories towards the refinements of design and fabrication of GaAs monolithic microwave integrated circuits (MMIC's). The trade-offs between RF performance and circuit design for chip size reduction and the choice of fabrication processes for better yield and reproducibility are major concerns in MMIC development .

Although distributed transmission lines such as microstrips are mostly used as matching circuit elements in MMIC amplifiers above C band , a lumped-element circuit approach is usually preferred in amplifiers below S band for flexibility and smaller chip size. In order to obtain a good input match, the hitherto reported amplifiers of a lumped-element design employ either a shunt resistor at the input port or a feedback resistor, at a sacrifice of noise figure[2],[3]. While MIM or interdigital capacitors are commonly used for the inter-stage DC-blocking in MMIC amplifiers[3], a direct-coupled scheme will be more effective for chip size reduction[4]. For incorporation of GaAs FETs, Schottky diodes and resistors into MMIC chips, ion-implantation technology is being considered as a most viable candidate instead of epitaxial processes.

We designed and fabricated a two-stage direct-coupled GaAs monolithic amplifier operating between 0.5 and 1.5GHz. In our design, the gate widths of FETs were tailored so as to minimize the noise figure to a 50Ω signal source impedance. Furthermore, a direct-coupled scheme was employed for chip size reduction. Selective ion-implantation was exclusively used for fabrication of circuit elements such as FETs . Schottky diodes and resistors to realize a planar structure and obtain uniformity and reproducibility. The following sections describe circuit design, device fabrication and RF performance.

Circuit Design

The amplifier was designed to give a good noise figure with adequate output match over 0.5 ~1.5GHz. A circuit diagram of the two-stage direct-coupled amplifier is shown in Fig.1. In order to pull up the source potential of second-stage FET, five series-connected diodes are inserted between the source and ground. The direct-coupled scheme is very effective to reduce the chip size. For example , an otherwise required inter-stage DC-block capacitor of ~20pF becomes unnecessary, thereby saving a pattern area 0.2mm^2 (450μm x 450μm) for a MIM capacitor fabricated using 4000Å thick SiO_2 film. The voltage pull-up diodes, on the other hand, can be fabricated with a pattern area of only 0.05mm^2. Input and output capacitors were not incorporated in the present amplifier design since they are not the essential prerequisite for our experimental purposes. In order to obtain a good noise figure and an adequate output match simultaneously, we tried to optimize the gate width of FETs by using computer simulations.

Prior to this, DC operating conditions of the FETs and diodes were determined according to the following procedures.

1. Let the dimensions of FET1 and FET2 identical.
2. Operate the FETs at a drain-source voltage V_{DS}=3.5V and a gate-source voltage V_{GS}=-1V.
3. Keep the source potential V_{S2} of FET2 at 4.5 V by connecting five Schottky barrier diodes in series between the source and the ground, thus the drain potential V_{D2} of FET2 being 8V.
4. Fix the DC-bias voltage V_{DD} of the amplifier to 12V, and determine the resistance of resistors R_1 and R_2 to bring the bias potentials of FETs as designed in accordance with the drain current of each FET.

RF performances such as noise figure, gain and input and output VSWR were calculated for various FET gate widths. A noise figure of a GaAs FET under a source impedance Z_0=50Ω is expressed by

$$F = F_{min} + \frac{R_n}{Z_0} \cdot \frac{(Z_0 - R_{op})^2 + X_{op}^2}{R_{op}^2 + X_{op}^2} \quad --(1)$$

where F_{min} is the minimum or optimum noise figure, R_n the equivalent noise resistance, and $Z_{op} = R_{op} + jX_{op}$ the optimum signal source impedance. The performance simulation was carried out in the

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following steps.

1. Noise parameters Fmin, R_n and Z_{op} were measured for a discrete GaAs FET with a gate length of 1μm and a gate width of 400μm fabricated using ion-implantation technology to be described later in this paper. Fmin of 0.8 dB and an associated gain of 12dB were obtained at V_{DS}=3.5V and the drain current I_D=16mA, R_n of 13.3Ω and Z_{op} of 25+j190Ω were also obtained.
2. From S-parameter measurements for frequencies from 0.5 to 4GHz, the equivalent circuit parameters of the 400μm gate width GaAs FET were calculated.
3. For varied gate width FETs with gate length kept unchanged, Fmin was assumed constant, and the values of R_n and Z_{op} were determined by scaling. The value of drain current and equivalent circuit parameters were also determined by scaling for varied gate width FETs.
4. Each pulling-up Schottky diode for FET2 was assumed to be operating at a DC terminal voltage of 0.9V and its differential resistance was assumed 7.5Ω for a DC current of 16mA. The junction area of the diode was adjusted by scaling for varied gate width FET.

Amplifier RF performances for various gate width FETs have been simulated at 1GHz. Fig.2 shows the calculated noise figure, gain and input and output return loss as a function of gate width W_g varing from 0.2 to 2mm. It can be seen that all the performances are improved by increasing W_g up to 1mm, but little improvement is achieved for W_g above 1mm except for output return loss. Thus, for our amplifier we determined the FET gate width to be 1mm and the values of resistor R_1 and R_2 to be 210Ω and 100Ω, respectively.

Fig.3 shows the calculated frequency response of the noise figure (NF), gain (G) and input and output return loss of the two stage amplifier with 1mm-width FETs. It is seen that NF≦2dB and G≧20 dB are obtainable in the frequency range 0.5~2GHz. At 1GHz, NF=1.1dB, G=26dB, and input and output return loss of 3dB and 13dB are predicted from the calculation.

Device structure and fabrication

The designed cross section of the direct-coupled MMIC fabricated using selective ion-implantation technology is schematically shown in Fig.4. The top view of the fabricated device is shown in Fig.5. The chip size is 1.5mm x 1.5mm x 300μm.

The gate length, width and finger length of the FETs are 1μm, 1000μm and 500μm, respectively. The gate electrodes are located in the center of the source and drain electrodes separated by 4μm. The peak carrier concentrations of active and contact layers are selected to 2 x $10^{17}cm^{-3}$ and 1 x $10^{18}cm^{-3}$, respectively.

The Schottky diode is composed of an implanted active layer with a carrier concentration of 1 x $10^{18}cm^{-3}$, Schottky barrier metal with a size of 160μm x 43μm and ohmic contact metal separated by 2μm from the edge of Schottky barrier metal. Five diodes are cascaded to pull up the source potential of FET2 to 4.5V.

Each resistor R_1 and R_2 is made of four series-connected resistor segments for provision of resistance adjustment if needed. The width and net total length of R_1 are patterned to be 150μm and 51μm and those of R_2 to be 180μm and 29μm. The designed sheet resistivity of resistor layers is 620Ω□.

For realizing a planar structure, selective ion-implantation technology was applied to make all the circuit elements. Silicon ions were implanted into qualified Cr-doped semi-insulating substrates. The substrate qualification was performed by quantitative analysis of Cr impurities and thermal conversion tests. A resist/SiO_2 film was used as a mask for selective ion-implantation.

The acceleration energy and dose are 70 keV and 3 x 10^{12} cm^{-2} for FET active layers, and 100 keV and 4 x 10^{12} cm^{-2} for resistor layers, respectively. For FET contact layers and Schottky diode layers, Si ions were dually implanted at a dose of 2 x 10^{13} cm^{-2} and energy of 250 and 120 keV. After ion-implantation and removal of the resist/SiO_2 film, the wafers were annealed at 850°C for 15 minutes in AsH_3 / Ar atmosphere without encapsulants. Figure 6 shows the carrier concentration profiles of these layers.

The Schottky barrier electrodes of FETs and diodes were formed by Al with thickness of 5000Å. Ohmic electrodes were formed by alloying Pt/AuGe at 450°C. Au/Pt/Ti metal systems were used for the bonding pads and interconnection. All of the metal layers were defined by a conventional photolithography and a lift-off process. The MMIC chips were glassivated by a CVD SiO_2 film except for the bonding area.

RF Performance

Fig.7 shows the circuit configuration for performance evaluation of the amplifier chip (surrounded by a dashed line). The chip was mounted in a coplanar waveguide test fixture. The source pad of FET1 which is connected to the cathode of the Schottky diode is grounded via bonding wires. Resistance adjustments of R_1 and R_2 by shunting the resistor segments via bonding wires were not done in the RF measurements.

RF measurements were performed with a 50Ω network analyzer system. The gate bias network and DC-block capacitor are externally connected at the input and output port of the test fixture. A 1000 pF capacitor is used for RF bypass at the DC bias terminal.

Fig.8 shows the measured frequency responses of the noise figure, gain and input and output return loss of the amplifier operated at V_G=-1V, V_{DD}=12V and the total drain current I_{DD}=90mA. Noise figures/gains of 0.8dB/27dB, 1.5dB/26dB and 1.9dB/21dB have been obtained at 0.5, 1.0 and 1.5 GHz, respectively. The input and output return losses have been measured to be 2.5dB (VSWR=7.0) and 15dB (VSWR=1.4) at 1GHz, respectively. The measured RF performances were in a good agreement with the simulation results shown in Fig.2. A slight gain

degradation above 1GHz might be caused by the capacitive parasitics of the resistors R_1 and R_2.

Fig. 9 shows the measured noise figure and gain as a function of gate voltage V_G for V_{DD}=12V at 1GHz . The noise figure and the gain are seen nearly constant for gate bias voltage $V_G \leqq -0.5V$. When V_G is increased above -0.5V, the gain drops rapidly accompanied by the noise figure degradation. This is caused by the beginning of pinch-off of FET2 due to the drain current increase of FET1 and the associated voltage drop increase across the resistor R_1.

Conclusion

Two-stage direct-coupled GaAs FET monolithic amplifiers operating at 1GHz-band have been developed. The noise figure of 2dB and the gain of over 20dB were obtained at frequencies from 0.3 to 1.5 GHz. Design optimization of FET gate width has been found effective in lowering noise figure for a signal source impedance of 50Ω. Direct-coupled scheme and the use of Schottky diodes for pulling up the source voltage of second-stage FET have been found successful for chip size reduction . Selective ion-implantation technique has been used throughout for the realization of planar MMICs.

Acknowledgment

The authors wish to thank M. Ohtomo and K. Mishima for continuous encouragement and helpful discussions.

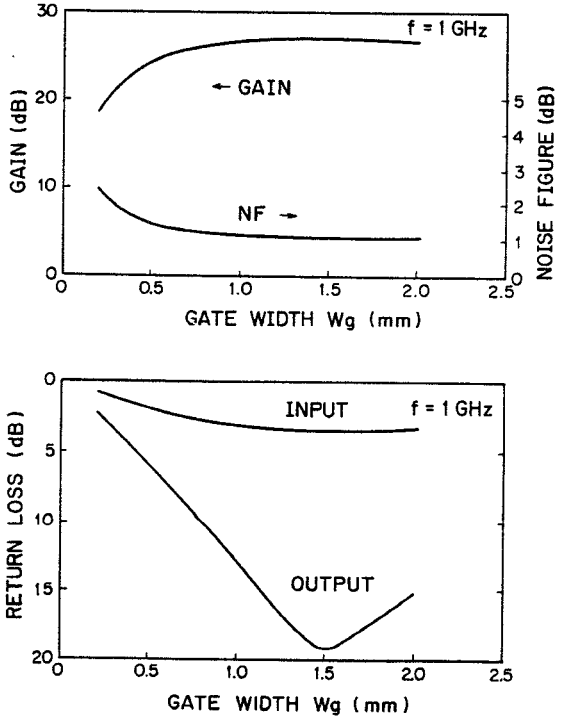

Fig. 2. Calculated amplifier RF performance at 1GHz as a function of gate width of FET.

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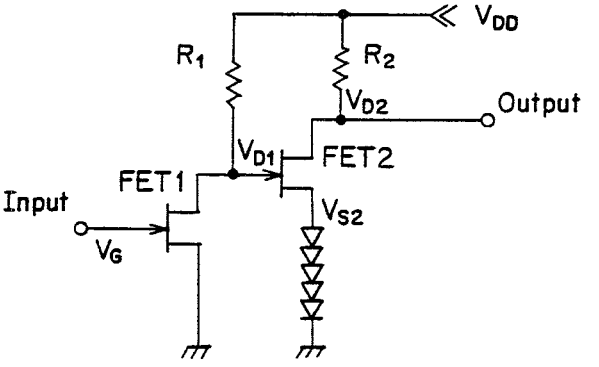


Fig. 1. Cirucuit diagram of direct-coupled MMIC amplifier.

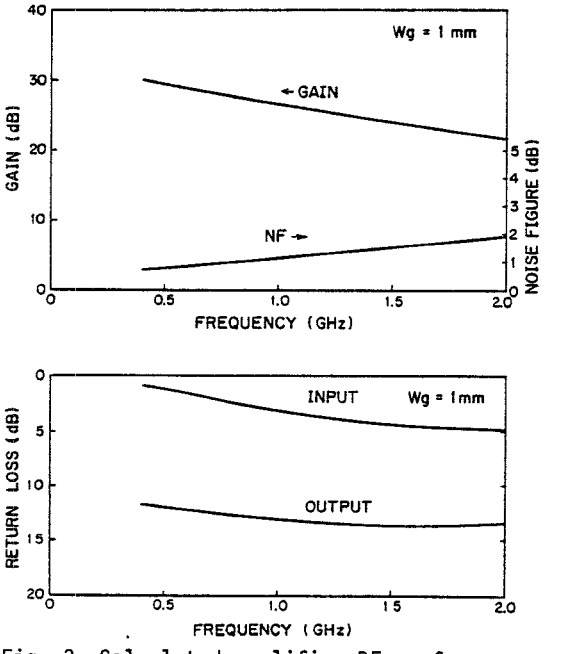


Fig. 3. Calculated amplifier RF performance as a function of frequency for FET with gate width of 1mm.

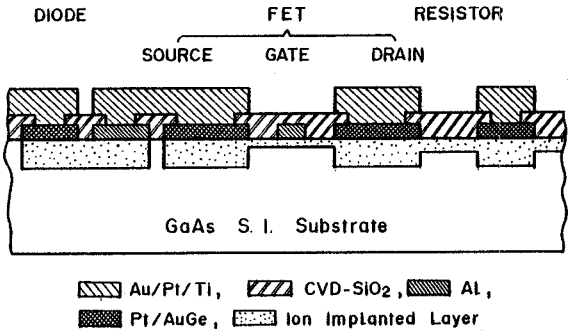


Fig. 4. Schematic cross section of MMIC chip.

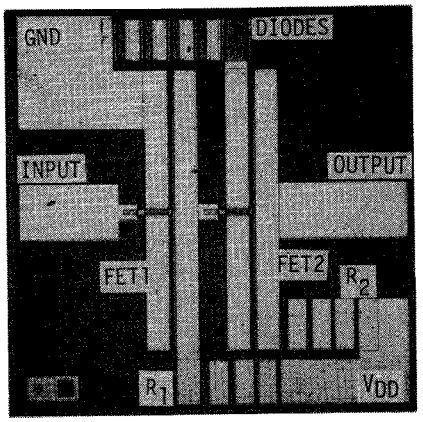


Fig. 5. Top view of MMIC chip.

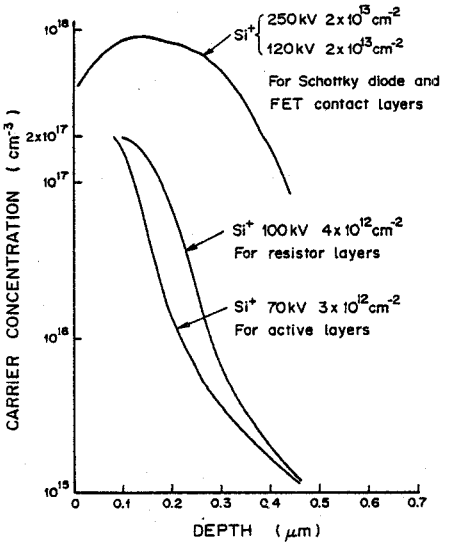


Fig. 6. Carrier concentration profiles of FET active and contact layers, resistor layers and Schottky diode layers.

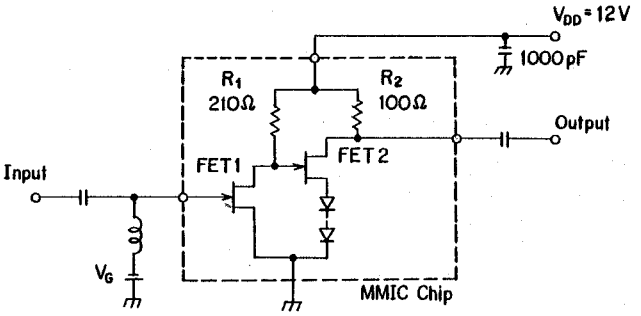
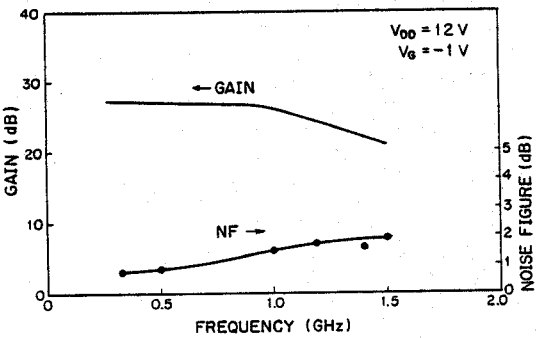


Fig. 7. Circuit configuration for MMIC amplifier evaluation.



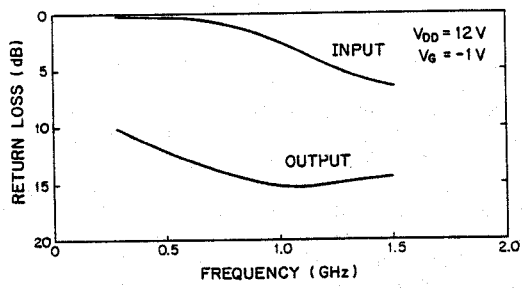


Fig. 8. Measured RF performance as a function of frequency for V_{DD}=12V and V_G=-1V.

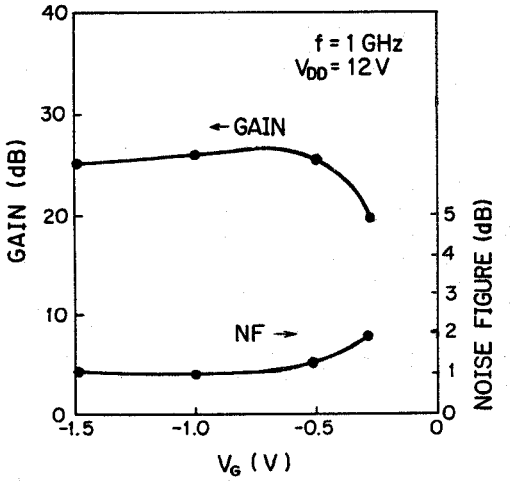


Fig. 9. Measured RF performance as a function of gate bias voltage V_G for V_{DD}=12V at 1GHz.